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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/615,841

07/10/2003

Hideto Hidaka

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9692

7590

09/15/2004

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EXAMINER

LE, THONG QUOC

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 09/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

20

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/615,841	HIDAKA, HIDETO	
	<b>Examiner</b>	<b>Art Unit</b>	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-17 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-6 and 14-17 is/are allowed.
- 6) ☒ Claim(s) 7-9 is/are rejected.
- 7) ☒ Claim(s) 10-13 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☒ All    b) ☐ Some    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. ____.  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____.  | 6) <input type="checkbox"/> Other: ____.                                    |

**DETAILED ACTION**

1. Claims 1-17 are presented for examination.

***Information Disclosure Statement***

2. This office acknowledges receipt of the following items from the Applicant:  
Information Disclosure Statement (IDS) filed on July 10, 2003.
3. Information disclosed and list on PTO 1449 was considered.

***Priority***

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Specification***

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The definition of the spare memory cells does not disclose.

8. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the arrangement between memory cells in claim 7, spare memory cells and normal memory cells in claim 8.

Claim should be amended for more clearly relationship between memory cells, normal memory cells and spare memory cells as disclosed in claim 8.

### ***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

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10. Claims 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Muranaka et al. (U.S. Pub. Patent No. 2002/0071308).

Regarding claims 7-8, Muranaka et al. disclose a memory device (Figure 10) comprising:

a plurality of memory cells (Figure 1) storing information by a change in respective electric resistance, and arranged in one memory cell array (Figure 1);

a read amplifying circuit (Figure 18, 511) performing parallel data reading from a plurality of selected memory cells (512) selected simultaneously among said plurality of memory cells; and

a current path forming section forming a plurality of read current paths respectively corresponding to said plurality of selected memory cells between said read amplifying circuit and a supply source of a power supply potential (ABSTRACT),

wherein said plurality of read current paths are separated from each other at least in said memory cell array (Figure 18, 512x2).

Regarding claim 9, Muranaka et al. disclose wherein said current path forming section includes: a plurality of source lines s giving reference potentials for data reading to each of said plurality of selected memory cells, and said plurality of source lines are separated from each other at least in the memory cell array (ABSTRACT).

***Allowable Subject Matter***

11. Claims 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-13 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Muranaka et al. (U.S. Patent No. 2002/0071308), and others, does not teach the claimed invention having a first and second source lines, among said plurality of source lines, provided correspondingly to said first and second selected memory cells are geometrically interchanged therebetween so that in a first respect region where said first memory cell is arranged, said first source line is placed along said first row and said second source line is placed along a second row adjacent to said first row, while in a second region where said second memory cell is arranged, said second source line is placed along said first row and said first source line is placed along said second row.

12. Claims 1-6, 14-17 are allowed.

Claims 1-6, 14-17 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Muranaka et al. (U.S. Patent No. 2002/0071308), and others, does not teach the claimed invention having a connecting circuit not only connects a first selected bit line among said plurality of bit lines to be selected according to a first input address to a first data line among said plurality of data lines, but also forms parts of paths that connect a part of said plurality of spare memory cells to be selected

according to said first input address to a second data line different from said first data line among said plurality of data lines, and also not only connects a second selected bit line among said plurality of bit lines to be selected according to a second input address to said second data line, but also forms parts of paths that connect a part of said plurality of spare memory cells to be selected according to said second input address to said first data line.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le  
Primary Examiner  
Art Unit 2818

**THONG LE**  
**PRIMARY EXAMINER**